

a horizontal scanning circuit for sampling the digital video data in the initial sequencing order;

a latch circuit for latching the sequenced digital video data synchronously with output from the horizontal scanning circuit; a D/A converter for converting the digital video data output from the latch circuit into analog signals;

plural signal transfer switches provided between D/A converter and plural signal lines; a transfer switch selection circuit for selecting at least one of said plurality of signal transfer switches to output the analog signal in the same order as the different sequencing order of the digital video data.

REMARKS

Claims 1, 2, 4, 5, 7-19, 21, 22, 24-38 and 49-51 are now presented for examination. Claims 1, 18 and 49 are the only independent claims. Claims 1, 18 and 49 have been amended to define still more clearly what Applicants regard as their invention.

Claim 49 was rejected under 35 U.S.C. § 112, second paragraph, as indefinite. Claim 49 has been amended and as amended is believed fully to comply with the provisions of Section 112, second paragraph. Withdrawal of the rejection is requested.

Claims 1, 2, 4, 5, 7-12, 15, 16, 18, 19, 21, 22, 24-29, 32, 33, 35, 38 and 49-51 were rejected under 35 U.S.C. § 103 as obvious from Lewis in view of Yamaguchi and Shinya. Claims 13, 14, 17, 30, 31, 34, 36 and 37 were rejected under 35 U.S.C. § 103 as obvious from Lewis in view of Yamaguchi and Shinya and further in view of Misawa.

Applicants respectfully traverse the rejections, and submit that the independent Claims 1, 18 and 49, together with the remaining claims dependent thereon, are patently distinct from the cited prior art for at least the following reasons.

Each of the independent claims recite, *inter alia*, a circuit for changing an initial sequencing order of the digital video data inputted through an input terminal into a different sequencing order, and for outputting the digital video data in the different sequencing order; as well as a selection circuit for selecting at least one of signal transfer switches to output analog signals in the same order as the different sequencing order of the digital video data.

Lewis shows a display driver architecture using D/A converters. Yamaguchi is relied upon as showing inverting analog signal polarity. Shinya is relied upon as showing the buffering of the analog signal. However, Applicants have found nothing in any of these cited references that teaches or suggests the advantageous feature of the independent claims discussed above.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

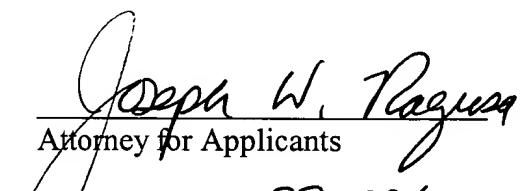
This Amendment After Final Rejection is believed clearly to place this application in condition for allowance and its entry is therefore believed proper under 37 C.F.R. § 1.116. At the very least, however, it is believed clear that the formal rejections have been overcome. Accordingly, entry of this Amendment After Final Rejection, as an

earnest effort to advance prosecution and reduce the number of issues, is respectfully requested.

In view of the foregoing remarks, Applicants respectfully request favorable reconsideration.

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE TO CLAIMS

1. (Five Times Amended) A matrix substrate having plural switching elements provided in matrix corresponding to intersecting points of scanning lines and signal lines, plural picture element electrodes connected to the switching elements, and horizontal circuits and vertical circuits for inputting the signals to the switching elements, the matrix substrate comprising:

an input terminal for inputting digital video data;

a circuit for [sequencing the digital video data inputted into said input terminal] changing an initial sequencing order of the digital video data inputted through said input terminal into a different sequencing order, and for outputting the digital video data in the different sequencing order;

a horizontal scanning circuit for sampling the digital video data in the [sequenced] initial sequencing order;

a latch circuit for memorizing the data synchronously with output from the horizontal scanning circuit;

a D/A converter for converting an output from the latch circuit into analog signals;

plural signal transfer switches provided between the D/A converter and the signal lines;

a selection circuit for selecting at least one of the signal transfer switches to output analog signals in the same [sequenced] order as the [sequenced] different sequencing order of the digital video data;

circuitry which inputs signal-polarity inverting signals together with the

picture data, and which inverts the polarity of the analog signal from the D/A converter; and
a buffer disposed between said D/A converter and said selection circuit,
which stores the analog signal of inverted polarity from the D/A converter,
wherein a number M of said D/A converters is less than a number N of
said switching elements arranged in a horizontal direction, and analog signals are sequentially
inputted from particular ones of said M D/A converters to N/M plural switching elements
arranged in a horizontal direction.

18. (Five Times Amended) A liquid crystal device comprising a matrix
substrate having plural switching elements provided in matrix corresponding to intersecting
points of scanning lines and signal lines, plural picture element electrodes connected to the
switching elements, and horizontal circuits and vertical circuits for inputting the signals to the
switching elements; a counter substrate opposing to the matrix substrate; and a liquid crystal
material placed between the matrix substrate and the counter substrate, the matrix substrate
comprising:

an input terminal for inputting digital video data;
a circuit for [sequencing the digital video data inputted into said input
terminal] changing an initial sequencing order of the digital video data inputted through said
input terminal into a different sequencing order, and for outputting the digital video data in the
different sequencing order;

a horizontal scanning circuit for sampling the digital video data in the
[sequenced] initial order;

a latch circuit for memorizing the data synchronously with output from the
horizontal scanning circuit;

a D/A converter for converting the output from the latch circuit into analog signals;

plural signal transfer switches provided between D/A converter and the signal lines;

a buffer disposed between said D/A converter and said plural signal transfer switches, which stores the analog signal of inverted polarity from the D/A converter;

a selection circuit for selecting at least one of the signal transfer switches to output analog signals in the same [sequenced] order as the [sequenced] different sequencing order of the digital video data; and

means for inputting signal-polarity inverting signals together with the picture data, and for inverting the polarity of the analog output of the D/A converter,

wherein a number M of said D/A converters is less than a number N of said switching elements arranged in a horizontal direction, and analog signals are sequentially inputted from particular ones of said M D/A converters to N/M plural switching elements arranged in a horizontal direction.

49. (Amended) A horizontal circuit comprising:

an input terminal for inputting digital video data;

a sequencing circuit for [sequencing the digital video data inputted into said input terminal] changing an initial sequencing order of the digital video data inputted through said input terminal into a different sequencing order, and for outputting the digital video data in the different sequencing order;

a horizontal scanning circuit for sampling the digital video data in the [sequenced] initial sequencing order;

a latch circuit for latching the sequenced digital video data synchronously with output from the horizontal scanning circuit;

a D/A converter for converting the digital video data output from the latch circuit into analog signals;

plural signal transfer switches provided between D/A converter and plural signal lines:

a transfer switch selection circuit for selecting at least one of said plurality of signal transfer switches to output the analog signal in the same [sequenced] order as the different sequencing order of the digital video data.